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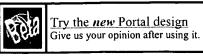
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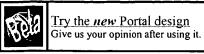
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A design for testability technique for RTL circuits using control/data flow extraction

Proceedings of the 1996 IEEE/ACM international conference on Computer-aided design January 1997

Indradeep Ghosh, Anand Raghunathan, Niraj K. Jha

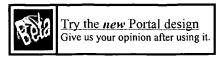
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Guidelines for creating a debuggable processor

80%

R. E. McLear , D. M. Scheibelhut , E. Tammaru

Proceedings of the first international symposium on Architectural support for programming languages and operating systems March 1982

Hardware without software is of little use. Systems that ease the task of debugging software reduce cost and speed development. This paper presents guidelines for designing processors that ease debugging for real-time computer systems. Special hardware can aid the debugging process by tracing execution and accesses to memory. Such hardware requires access to signals that may not be readily available. Other, less exotic hardware provides an interface to the programmer and other processors. T ...

A structural view of the Cedar programming environment

80%

Daniel C. Swinehart , Polle T. Zellweger , Richard J. Beach , Robert B. Hagmann

ACM Transactions on Programming Languages and Systems (TOPLAS) August 1986

Volume 8 Issue 4

This paper presents an overview of the Cedar programming environment, focusing on its overall structure—that is, the major components of Cedar and the way they are organized. Cedar supports the development of programs written in a single programming language, also called Cedar. Its primary purpose is to increase the productivity of programmers whose activities include experimental programming and the development of prototype software systems for a high-performance personal computer. T ...

IS '97: model curriculum and guidelines for undergraduate degree programs in information systems

80%

Gordon B. Davis , John T. Gorgone , J. Daniel Couger , David L. Feinstein , Herbert E. Longenecker

ACM SIGMIS Database, Guidelines for undergraduate degree programs on Model curriculum and guidelines for undergraduate degree programs in information systems December 1997

Volume 28 Issue 1

A user's viewpoint on the Programmer's Workbench

77%

M. H. Bianchi, J. L. Wood

Proceedings of the 2nd international conference on Software engineering October 1976

The Programmer's Workbench boasts a broad set of highly useful features aimed at the application program developer. It claims to be a "human-end" computer providing tools and services to ease the load on the application system designer, programmer, documenter, tester, and delivery personnel. This paper shows the benefits of using the PWB tools, individually and in combination. Through specific examples drawn from the history of a software project, evidence is given that the use ...

Simulating modular microcomputers

77%

Frank J. Langley , Gerald A. LaGro , Joan Sheehan Proceedings of the eleventh annual simulation symposium March 1978

The commitment of microprocessor-based system configurations to detailed logic design and breadboard fabrication traditionally results in a costly development cycle. This paper reports on the use of a computer design high-order-language (HOL) to simulate micro-computer functional elements, "macromodules", at the register level, and verify the timing and interface requirements for a family of microcomputer configurations. The definitions of these microcomputer macromodules (i. e. ...



switch level. To allow the simulation of an entire system or check the correctness of a single circuit, the different modeling techniques can

be easily intermixed. THEMIS is a highly interactive simulator ...

12 Supporting reference and dirty bits in SPUR's virtual address cache

D. A. Wood , R. H. Katz ACM SIGARCH Computer Architecture News, Proceedings of the 16th annual international symposium on Computer architecture

April 1989 Volume 17 Issue 3

Virtual address caches can provide faster access times than physical address caches, because translation is only required on cache misses. However, because we don't check the translation information on each cache access, maintaining reference and dirty bits is more difficult. In this paper we examine the trade-offs in supporting reference and dirty bits in a virtual address cache. We use measurements from a uniprocessor SPUR prototype to evaluate different alternatives. The prototype's buil ...

13 Distributed operating systems

Andrew S. Tanenbaum, Robbert Van Renesse

ACM Computing Surveys (CSUR) December 1985

Volume 17 Issue 4

Distributed operating systems have many aspects in common with centralized ones, but they also differ in certain ways. This paper is intended as an introduction to distributed operating systems, and especially to current university research about them. After a discussion of what constitutes a distributed operating system and how it is distinguished from a computer network, various key design issues are discussed. Then several examples of current research projects are examined in some detail ...

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14 4	Statemate: a working environment for the development of complex reactive systems D. Harel , H. Lachover , A. Naamad , A. Pnueli , M. Politi , R. Sherman , a. Shtul-Trauring Proceedings of the 10th international conference on Software engineering April 1988 This paper provides a brief overview of the STATEMATE system, constructed over the past three years by i-Logix Inc., and Ad Cad Ltd. STATEMATE is a graphical working environment, intended for the specification, analysis, design and documentation of large and complex reactive systems, such as real-time embedded systems, control and communication systems, and interactive software. It enables a user to prepare, analyze and debug diagrammatic, yet precise, descriptions of the system under devel	77%
15 4	Monitoring and performance measuring distributed systems during operation D. Wybranietz, D. Haban Proceedings of the 1988 ACM SIGMETRICS conference on Measurement and modeling of computer systems May 1988 This paper describes an integrated tool for monitoring distributed systems continuously during operation. A hybrid monitoring approach is used. As special hardware support a test and measurement processor (TMP) was designed, which is part of each node in an experimental multicomputer system. Each TMP runs local parts of the monitoring software for its node, while all the TMPs are connected to a central test station via a separate TMP interconnection network. The monitoring system is transpa	77%
16 4	The fuzzball D. L. Mills ACM SIGCOMM Computer Communication Review , Symposium proceedings on Communications architectures and protocols August 1988 Volume 18 Issue 4 The Fuzzball is an operating system and applications library designed for the PDP11 family of computers. It was intended as a development platform and research pipewrench for the DARPA/NSF Internet, but has occasionally escaped to earn revenue in commercial service. It was designed, implemented and evolved over a seventeen-year era spanning the development of the ARPANET and TCP/IP protocol suites and can today be found at Internet outposts from Hawaii to Italy standing watch for adventurou	77%
17 ₫	Structured Programming with go to Statements Donald E. Knuth ACM Computing Surveys (CSUR) December 1974 Volume 6 Issue 4	77%
18 4	The evolution of the Sperry Univac 1100 series: a history, analysis, and projection B. R. Borgerson , M. L. Hanson , P. A. Hartley Communications of the ACM January 1978 Volume 21 Issue 1 The 1100 series systems are Sperry Univac's large-scale mainframe computer systems. Beginning with the 1107 in 1962, the 1100 series has progressed through a succession of eight compatible computer models to the latest system, the 1100/80, introduced in 1977. The 1100 series hardware architecture Is based on a 36-bit word, ones complement structure which obtains one operand from storage and one from a high-speed register, or two operands from high-speed registers. The 1100 Operating System	77%
19 বি	On the emulation of flowcharts by decision tables Art Lew Communications of the ACM December 1982 Volume 25 Issue 12 Any flowchart can be emulated by a decision table, whose complexity depends on that of the flowchart. It may be necessary, however, to introduce a new control variable with associated tests and sets or to permit changes in execution sequences provided action-test independence holds. Two measures of decision table complexity are discussed and interrelated. Finally, conditions and procedures for reducing complexity are presented.	77%
20 र	Development and application of NASA's first standard spacecraft computer Charles E. Trevathan , Thomas D. Taylor , Raymond G. Hartenstein , Ann C. Merwarth , William N. Stewart Communications of the ACM September 1984 Volume 27 Issue 9 To provide the autonomy needed by low, earth-orbiting satellites, NASA's first standard on-board processor requires changing only interfacing hardware from mission to mission.	77%

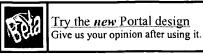
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systems being traced. In the past, researchers have collected instruction traces through various techniques, including single-stepping, instruction inlining, hardware monitoring, and processor simulation. These approaches, however, fail to produce accurate traces because they interfere with the processor's normal execution. Because processors are deterministic ...

24 Automatic performance prediction to support cross development of parallel programs Matthias Schumann

Proceedings of the SIGMETRICS symposium on Parallel and distributed tools January 1996

25 The performance impact of flexibility in the Stanford FLASH multiprocessor

Mark Heinrich , Jeffrey Kuskin , David Ofelt , John Heinlein , Joel Baxter , Jaswinder Pal Singh , Richard Simoni , Kourosh Gharachorloo , David Nakahira , Mark Horowitz , Anoop Gupta , Mendel Rosenblum , John Hennessy

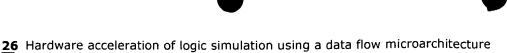
Proceedings of the sixth international conference on Architectural support for programming languages and operating systems November 1994

Volume 29, 28 Issue 11, 5

A flexible communication mechanism is a desirable feature in multiprocessors because it allows support for multiple communication protocols, expands performance monitoring capabilities, and leads to a simpler design and debug process. In the Stanford FLASH multiprocessor, flexibility is obtained by requiring all transactions in a node to pass through a programmable node controller, called MAGIC. In this paper, we evaluate the performance costs of flexibility by comparing the performance of ...

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G. Catlin, B. Paseman

ACM SIGMICRO Newsletter, Proceedings of the 18th annual workshop on Microprogramming December 1985

Volume 16 Issue 4

Current digital logic simulators running on engineering workstations lack capacity and speed. This paper discusses a hardware accelerator for a workstation simulator which addresses these problems. The accelerator runs 100x faster than its software counterpart and can simulate up to 1 million gates. The accelerator has been built and is being sold commercially. The architecture of the accelerator is similar to that of a classical dataflow machine. We describe the architecture of the machine ...

27 Launching the new era

77%

Kazuhiro Fuchi, Robert Kowalski, Koichi Furukawa, Kazunori Ueda, Ken Kahn, Takashi Chikayama, Evan Tick

Communications of the ACM March 1993

Volume 36 Issue 3

28 Efficient data breakpoints

77%

Robert Wahbe

ACM SIGPLAN Notices, Proceedings of the fifth international conference on Architectural support for programming languages and operating systems September 1992

Volume 27 Issue 9

77%

29 Personal distributed computing: the Alto and Ethernet hardware

Chuck Thacker

Proceedings of the ACM Conference on The history of personal workstations January 1986

Between 1972 and 1980, the first distributed personal computing system was built at the Xerox Palo Alto Research Center. The system was composed of a number of Alto workstations connected by an Ethernet local network. It also included servers that provided centralized facilities. This paper describes the development of the hardware that was the basis of the system.

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